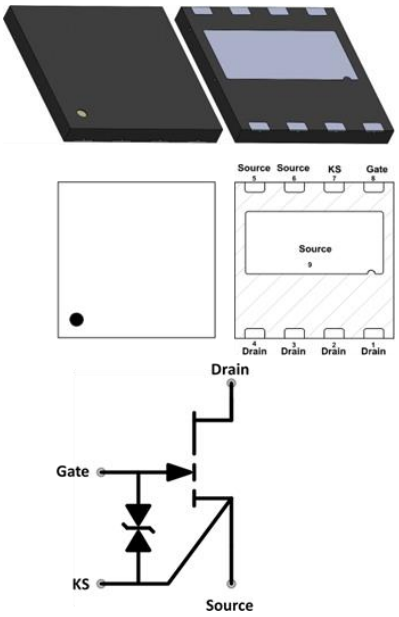
NW6507EBD8

GaN E-Mode 650V Power Transistor



Features

- 650 V enhancement mode GaN power transistor
- DFN 8x8 package
- Typical $R_{DS(on)}$ = 73 mΩ
- $I_{DS\ max,DC}$ = 27 A
- Simple gate drive 0 V to 6 V and large $V_{GS(th)}$
- High switching frequency (> 1 MHz)
- Reverse conduction capability
- Zero reverse recovery loss
- Kelvin Source for optimized gate drive
- Gate ESD protection

Applications

- PD chargers
- Power Adapters
- Power Factor Correctors
- High density power converters
- High efficiency power converters

Description

The NW6507EBD8 is an enhancement mode GaN transistor designed for large power density and high switching frequency. Its large threshold voltage and the presence of a kelvin source connection enable fast and safe gate driving. These features enable high efficiency and reliable power switching.

Pin Description

Pin Name	Description
8	Gate
1,2,3 4	Drain
5,6,9	Source
7	Kelvin Source

Absolute Maximum Ratings

T_J = 25 ˚C except as noted. Exceeding the maximum ratings may damage the device.

Parameter	Symbol	Value	Unit
Drain-to-Source Voltage	V_{DS}	650	V
Drain-to-Source pulse Voltage	V_{DS}(pulse)	800	V
Gate-to-Source Voltage	V_{GS}	-10 to +7	V
Gate-to-Source pulse Voltage	$V_{GS,pulse}$	8.5	V
Continuous drain current (T_C = 25 ˚C)	I_D	27	A
Pulsed drain current (T_C = 25 ˚C, T_{PULSE} = 1 µs)	$I_{D,pulse}$	78.8	A
Power dissipation	P_{tot}	107	W
Operating Junction Temperature	T_J	-55 to +150	˚C
Storage Temperature Range	T_S	-55 to +150	˚C

Thermal Characteristics

Parameter	Symbol	Value	Unit
Thermal Resistance, Junction to Case	$R_{TH,J-C,bottom}$	1.17	˚C/W
Thermal Resistance, Junction to Ambient	$R_{TH,J-A}$	46	˚C/W
Maximum reflow soldering temperature	T_{sold}	260	˚C

Electrical Characteristics

Static Characteristics

Parameters	Symbol	Min	Typ	Max	Unit	Condition
Drain-to-Source On Resistance	$R_{DS(on)}$	-	75	-	mΩ	I_{DS} = 8 A, V_{GS} = 6 V, T_J = 25 ˚C
		-	73	-	mΩ	I_{DS} = 8 A, V_{GS} = 7 V, T_J = 25 ˚C
		-	153	-	mΩ	I_{DS} = 8 A, V_{GS} = 7 V, T_J = 150 ˚C
Gate-to-Source Threshold Voltage	$V_{GS(th)}$	1.0	1.82	2.6	V	I_{DS} = 4.6 mA, T_J = 25 ˚C

		-	1.91	-	V	I_{DS} = 4.6 mA, T_J = 150 ˚C
Gate-to-Source Forward Leakage	I_{GSS}	-	1	-	mA	V_{GS} = 7 V, V_{DS}=0V,T_J = 25 ˚C
Drain-to-Source Leakage Current	I_{DSS}	-	1	-	µA	V_{DS}=650 V, V_{GS}=0 V, T_J = 25 ˚C
		-	50	-	µA	V_{DS}=650 V, V_{GS}=0 V, T_J = 150 ˚C

Dynamic Characteristics

Input Capacitance	C_{ISS}	-	139	-	pF	V_{DS} = 400 V, V_{GS} = 0 V, f = 1MHz
Output Capacitance	C_{OSS}	-	33.7	-	pF	
Reverse Transfer Capacitance	C_{RSS}	-	0.06	-	pF	
6Effective Output Capacitance, Energy-Related	$C_{O(ER)}$	-	49.7	-	pF	V_{DS} = 0 V to 400 V, V_{GS} = 0 V
Effective Output Capacitance, Time-Related	$C_{O(TR)}$	-	73.7	-	pF	
Output Charge	Q_{OSS}	-	29.3	-	nC	V_{DS} = 0 V to 400 V, V_{GS} = 0 V
Gate resistance	R_G	-	1.8	-	Ω	f = 100MHz, open drain

Gate Charge Characteristics

Total Gate Charge	Q_G	-	2.21	-	nC	V_{DS} = 400 V, I_D= 8 A, V_{GS} = 0 to 7V
Gate-to-Source Charge	Q_{GS}	-	0.34	-	nC	
Gate-to-Drain Charge	Q_{GD}	-	1.05	-	nC	
Gate plateau voltage	$V_{plateau}$	-	2.35	-	V	

Reverse conduction characteristics

Pulsed current, reverse	$I_{s,\ pulse}$	-	-	78.8	A	T_C = 25 ˚C
Source-Drain Reverse Voltage	V_{SD}	-	2.69	-	V	I_{SD} = 8 A, V_{GS} = 0 V, T_J = 25 ˚C
Reverse recovery chart	Q_{rr}	-	0	-	nC	Excluding Qoss
Reverse recovery time	T_{rr}	-	0	-	nS	-

Electrical Performance Graphs

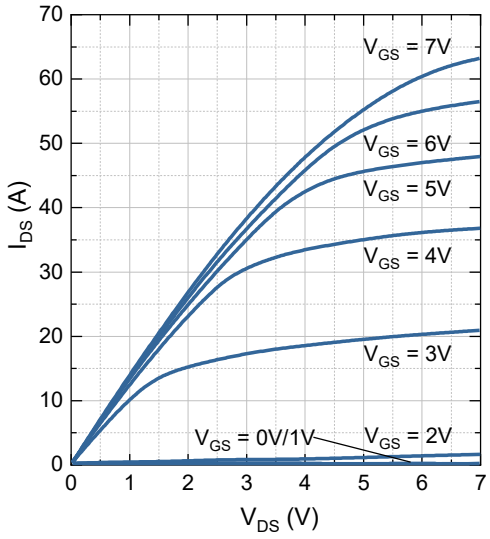


Figure 1: Typical pulsed I_{DS} vs. V_{DS} Output Characteristics at T_J = 25 ˚C

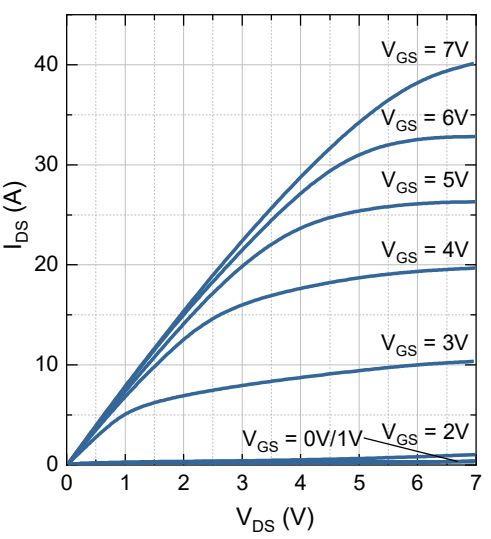


Figure 2: Typical pulsed I_{DS} vs. V_{DS} Output Characteristics at T_J = 125 ˚C

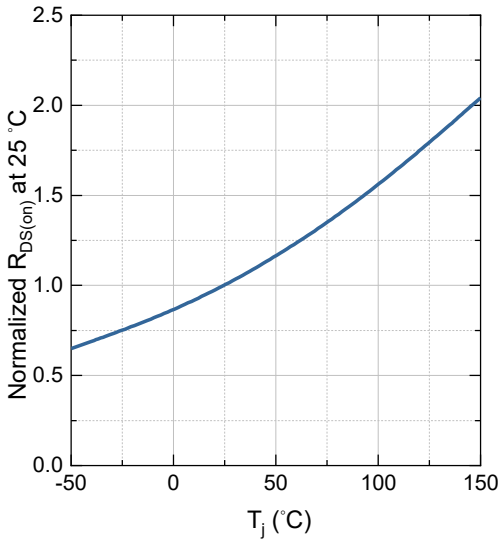


Figure 3: Normalized $R_{DS(on)}$ as a function of T_J

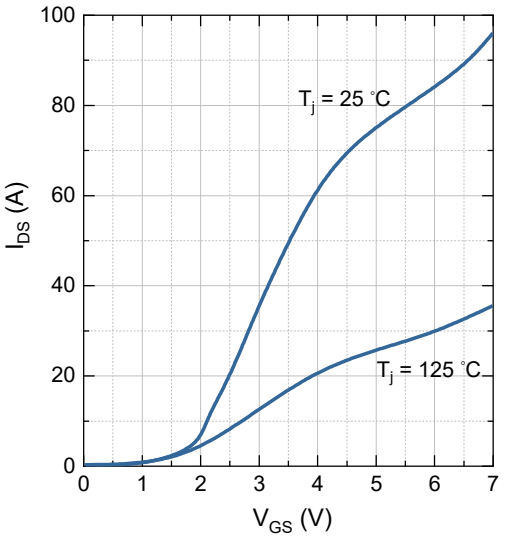


Figure 4: Typical I_{DS} vs. V_{GS} at T_J = 25 ˚C and T_J = 125 ˚C

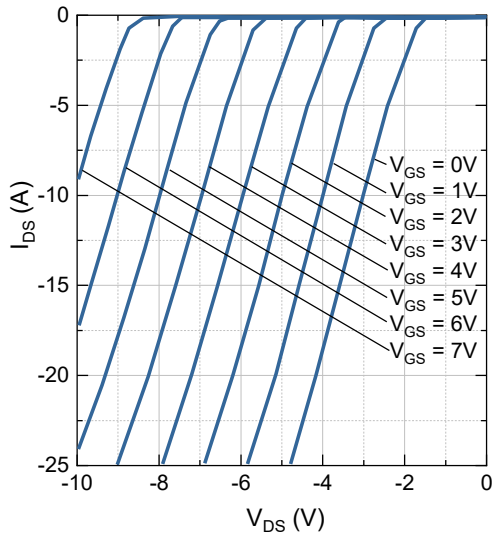


Figure 5: Typ. channel reverse characteristics (T_J =25°C)

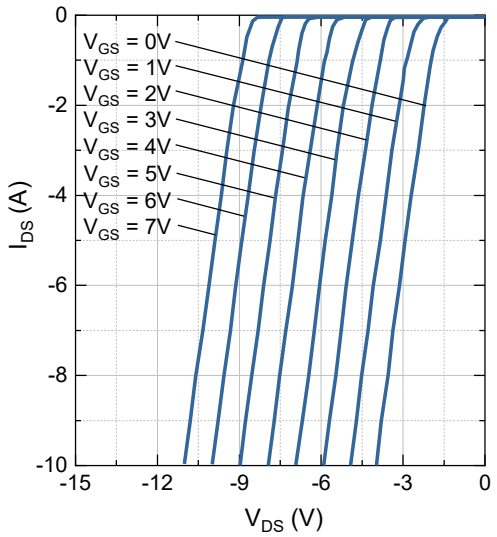


Figure 6: Typ. channel reverse characteristics (T_J =125°C)

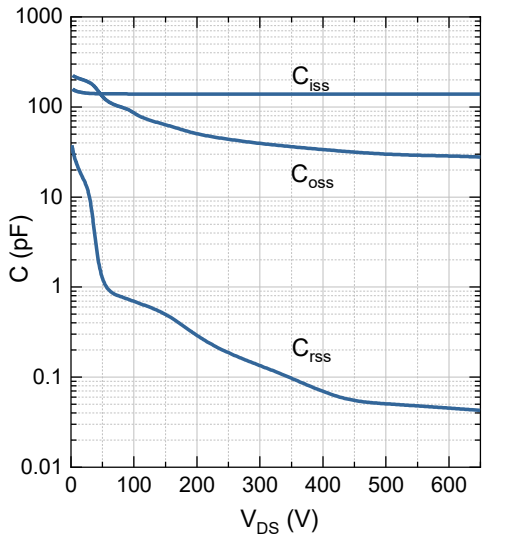


Figure 7: Typical C_{iss}, C_{oss}, C_{rss} vs. V_{DS}

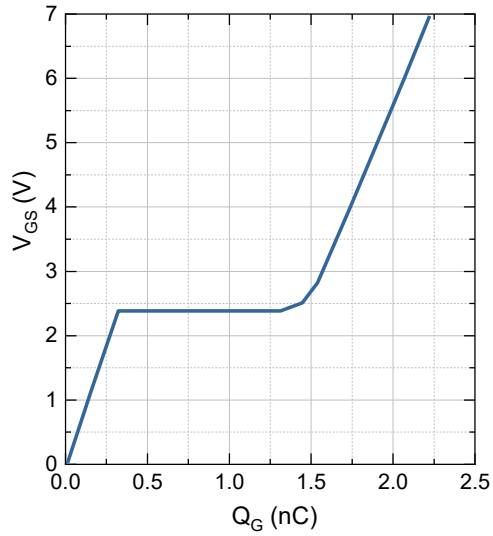


Figure 8: Typical V_{GS} vs. Q_G at V_{DS} = 400 V

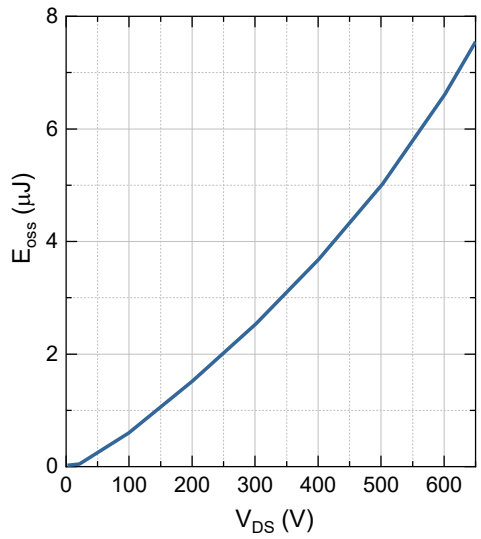


Figure 9: Typical energy stored in C_{oss}

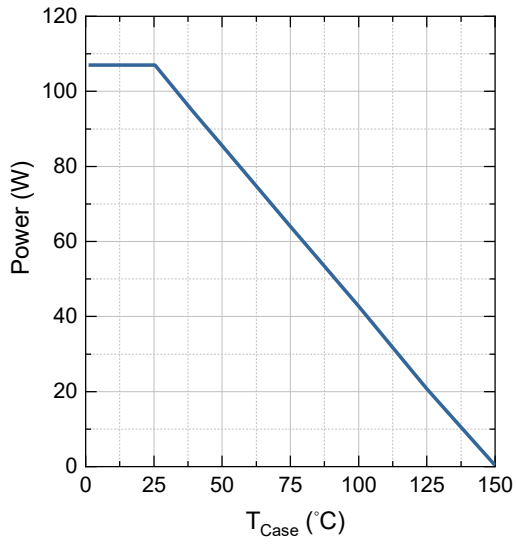


Figure 10: Power Derating vs. T_{case}

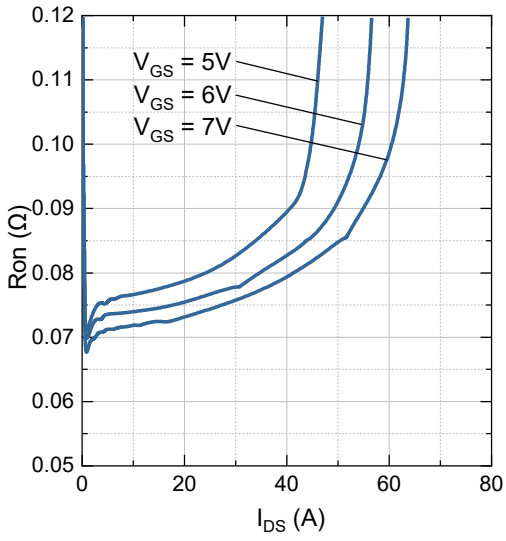


Figure 11: Typ. Drain-source on-state resistance

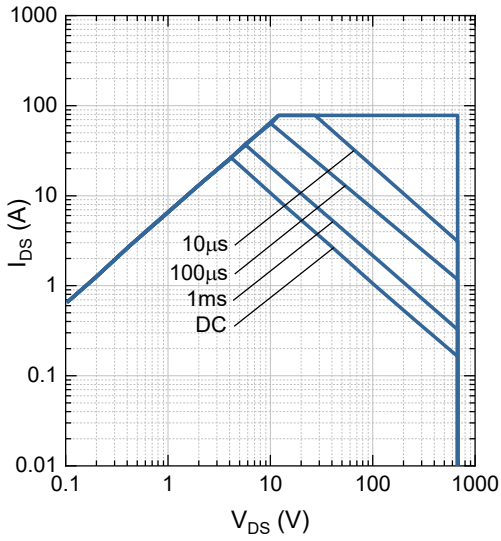


Figure 12: Safe operating area Tc=25°C

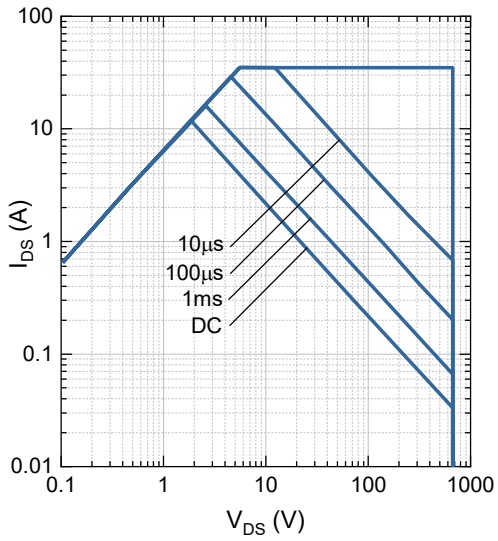


Figure 13: Safe operating area Tc=125°C

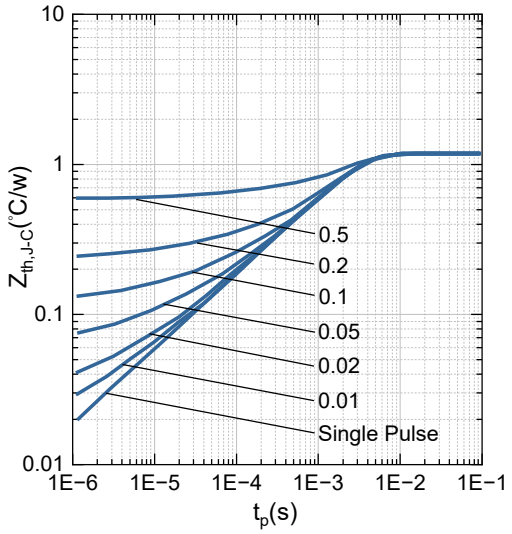
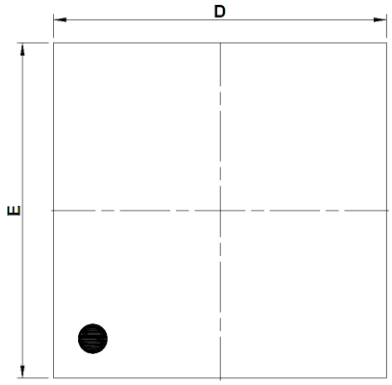


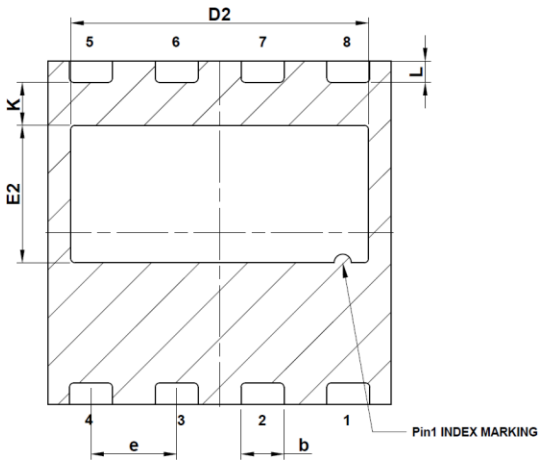
Figure 14: Max. Transient Thermal Impedance

Package Information

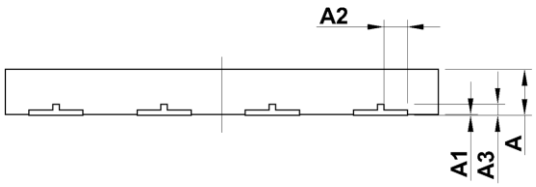
Top View

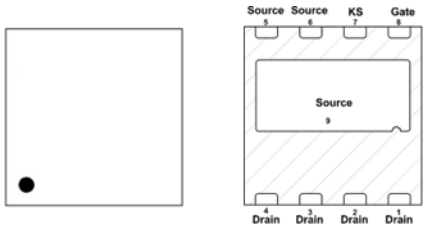


Bottom View



Side View

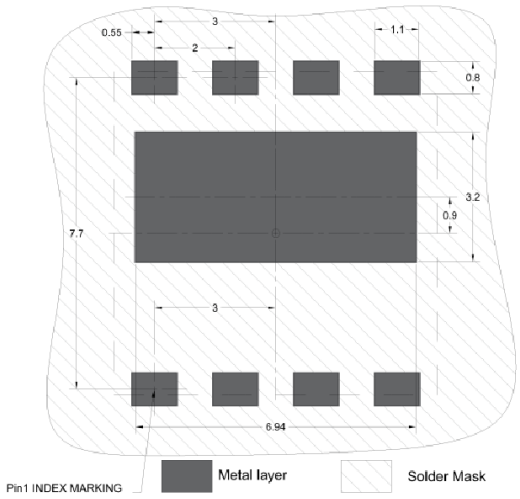




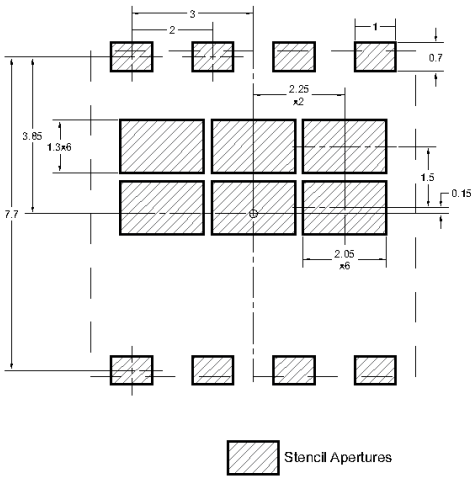
SYMBOLS	DIMENSIONS IN MILLIMETERS		
	MIN.	NOM.	MAX.
A	0.75	0.85	0.95
A1	0.00	0.02	0.05
A2	0.44 REF		
A3	0.203 REF		
b	0.95	1.00	1.05
D	7.90	8.00	8.10
D2	6.84	6.94	7.04
E	7.90	8.00	8.10
E2	3.10	3.20	3.30
e	2.00 REF		
K	1.00 REF		
L	0.45	0.50	0.55

Recommended PCB Footprint & Stencil

Recommended PCB Footprint



Recommended Stencil apertures



All dimensions are in units mm.
All pads are solder mask define.
Thickness of stencil : 100 µm

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